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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,234	07/09/2003	Shigeki Tomishima	009683-469	8323

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BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, VA 22313-1404

EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,234	TOMISHIMA ET AL.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/9/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This final Office action is in response to the amendment filed 01 November 2005. Claims 1-4 are pending. All objections and rejections not repeated below are withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Dreibelbis et al. [U.S. 5,875,470].

As to claim 1, Dreibelbis et al. discloses a memory device (Figure 1A; Figure 1B; Figure 2) comprising a memory unit (Bank 1.1-4.4 in Figure 1A) and an arbiter (combination of Bank Address Control 10 in Figure 1A, Crosspoint Switch 20 in Figure 1B, and I/O Selection Control 21 in Figure 1B) arbitrating (controlling/switching) bus (Address 16, Figure 1A; 5-1 to 5-4, Figure 1A) access requests (Column 5, lines 57-60; Column 6, lines 15-24; Column 2, lines 57-67) from a plurality of units (Figure 3; Column 6, lines 15-16), wherein an activation of the memory takes place before the end of the first access (Column 5, lines 2-5).

Thus, Dreibelbis et al. reasonably appears to disclose every limitation of claim 1 and therefore anticipates the claim within the meaning of 35 U.S.C. 102.

As to claim 2, Dreibelbis et al. already discloses a memory device wherein multiple bus accesses and data transfers from a plurality of units to the memory take place in parallel (Column 1, lines 9-12; Column 2, lines 6-20). It is therefore inherently understood that sending the requested data in response to the second access request to the unit making the request before the end of the first access is an acknowledgement to the second access request.

As to claim 3, Dreibelbis et al. discloses a plurality of memory banks (Column 2, lines 6-9; Column 4, lines 57-60; Figure 1A; Figure 2) in the disclosed memory device. The arbiter of the memory device has a plurality of address ports (Items 10, 11-1 to 14-4, Figure 1A) corresponding to a plurality of units (Column 2, lines 17-20; Column 4, line 64 to Column 5 line 5; Column 5, lines 27-36; Column 6, lines 15-20). Furthermore, the arbiter outputs an address for the second bus access request in parallel with the first access to a first bank (Column 5, lines 61-65), in order to activate a second memory bank (Column 5, lines 2-5).

Thus, Dreibelbis et al. reasonably appears to disclose every limitation of claim 3 and therefore anticipates the claim within the meaning of 35 U.S.C. 102.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dreibelbis et al., further in view of Masuoka et al. [U.S. 6,472,714].

As for claim 4, Dreibelbis et al. substantially discloses the memory device as described above, but does not teach a memory device that contains the units that make the bus access requests. However, it is obvious to one ordinarily skilled in the art at the time of the applicant's invention that a single chip embedded system such as System-on-Chip (SoC) has the advantages of higher performance, less power consumption, better reliability, and lower cost. Therefore, Dreibelbis et al.'s memory device would benefit from these advantages by making it a single chip device containing the units that make the bus access requests. Furthermore, Masuoka et al. teaches a SoC device that comprises memory and a plurality of units including a CPU for controlling the operation of the memory, and the increased degree of integration of the SoC device resulted in reduced area and improved operating speed (Column 1, lines 8-22). It would have been obvious to one ordinarily skilled in the art at the time of the applicant's invention that Dreibelbis et al.'s memory device would have improved operating speed and reduced area if it contained the plurality of units.

Response to Arguments

Applicant's arguments filed on 01 November 2005 have been fully considered but they are not persuasive.

In the first argument, on pages 5 (second paragraph) and 6 (first paragraph) of the amendment, Applicant argues that "Dreibelbis et al merely discloses that if a next

processor request is received while a bank has an active request, the next request must wait in control 10 until the required bank becomes available, which happens when it completes its current request. Thus, nothing in Dreibelbis et al shows, teaches or suggests that when a second bus access request takes place before a first bus access has been completed, the arbiter performs activation of the memory unit of the second bus request in parallel with the access to the memory unit of the first bus request as claimed in claim 1."

However, in the 102(b) rejection of claim 1 in the previous Office action, the examiner clearly stated that a memory unit is interpreted as the combination of the memory banks (Banks 1.1-4.4 in Figure 1A) instead of a single memory bank (as interpreted in Applicant's first argument), and it is clear in the prior art that when a second bus access request takes place before a first bus access has been completed, the arbiter performs activation of the memory unit that corresponds to the second bus access request in parallel with the access to the memory unit that corresponds to the first bus access request (Column 5, Lines 2-5; Column 5, Lines 61-63; Column 6, Lines 25-31). The prior art also recites, in numerous places, that Dreibelbis et al.'s memory device allows simultaneous accesses by multiple processors to multiple memory banks (Column 4, Lines 64-67; Column 5, Lines 1-5) . If there are simultaneous accesses to the memory banks, then the memory unit must be activated by the arbiter in response to the second request before the first access has been completed.

In the second argument, on page 6, second paragraph of the amendment, Applicant argues that "Dreibelbis et al. merely discloses bank address control 10 which

receives memory addresses requested by processors and simultaneously provides addresses on buses for selecting drivers of the banks."

However, Dreibelbis et al. clearly states, as described in the previous Office action (in column 6, lines 20-24, also cited by Applicant in the first argument) that if a next request is received by a bank while it has an active request, the next request must wait in control 10 until the required bank becomes available, and this clearly indicates that a form of arbitration is taking place at the arbiter (combination of Bank Address Control 10 in Figure 1A, Crosspoint Switch 20 in Figure 1B, and I/O Selection Control 21 in Figure 1B, as cited in the previous Office action). Since the access to data bus is a direct result of access to the memory bank, and the second request must be held back in favor of the first active request, thereby preventing the second request from accessing the requested memory bank and the data bus (one of 5-1 to 5-4 in Figure 1A, as cited in the previous Office action) connected to the memory bank. The prior art also cites (in Column 6, Lines 55-62) that only one to four banks may be simultaneously making transfers on the data buses during a transfer cycle, even though (in Column 6, Lines 25-31) all 16 banks can be busy at the same time, implying that there could be 16 concurrent chip accesses (in Column 5, Lines 1-5, the prior arts indicates that all 16 banks can be accessed concurrently since plural addresses can be provided on buses 11-1 through 11-4) while there are only four data buses, since there is only one data bus connected to each chip section, which is another indication of the presence of bus access arbitration. The prior art also cites (in Column 8, Lines 28-31) that the same processor can concurrently access banks in different chip sections. Therefore, if

multiple processors can access multiple banks in parallel, and there could be 16 simultaneous accesses to all 16 banks in the prior art, and a same processor can concurrently access banks in different chip sections, while only one to four data transfers can take place in the same transfer cycle, then a data bus arbitration scheme (Column 7, Lines 23-31 further supports that up to four banks are selected for data transfer for each transfer cycle, while there could be up to four competing accesses in each chip section) must exist to prevent the up to four bank accesses in the same chip section to access the associated data bus simultaneously, thereby reinforcing the Examiner's argument that Dreibelbis et al. does teach an arbiter which arbitrates for bus access requests since the arbiter (combination of Bank Address Control 10 in Figure 1A, Crosspoint Switch 20 in Figure 1B, and I/O Selection Control 21 in Figure 1B) resolves competing demands for a resource (in this case the memory bank and the associated data bus) by multiple access requests.

Since the Applicant argued the Examiner's rejections of claims 2-4 based purely on the Applicant's argument of claim 1, the Examiner gives no further argument regarding claims 2-4. Therefore all rejections are maintained and made final.

Conclusion

The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Patent No:

U.S. 6,321,284 B1	Multiprocessor System with Multiple Memory Buses for Access to Shared Memories
U.S. 5,937,204A	Dual-pipeline architecture for enhancing the performance of graphics memory
U.S. 6,173,356 B1	Multi-port DRAM with integrated SRAM and systems and methods using the same
U.S. 5,687,131 A	Multi-Mode Cache Structure

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Assistant Examiner
Art Unit 2189

15 November 2005

KEVIN VERBRUGGE
PRIMARY EXAMINER